R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 2, 4, 5, 9-15, 19 and 20 under 35 U.S.C. §102(b) as being anticipated by Orr has been obviated by appropriate amendment and should be withdrawn.

The rejection of claims 1, 2, 4, 5, 9-15, 19 and 20 under 35 U.S.C. §102(b) as being anticipated by Fletcher has been obviated by appropriate amendment and should be withdrawn.

Orr teaches an architecture for a distributive microprocessing system (Title). Fletcher teaches a multiprocessing system including a shared cache (Title).

In contrast, claim 1 of the present invention provides an apparatus comprising a system bus, a shared memory and a multiprocessor logic circuit. The shared memory may be (i) coupled to the system bus and (ii) configured to store data. The multiprocessor logic circuit generally comprises (i) a plurality of processors and (ii) a message circuit further comprising a message pipe-line FIFO. The message circuit is directly connected to the system bus and configured to pass messages between the plurality of processors. Each of the plurality of processors is directly connected to the system bus and configured to access the shared memory and the message circuit through the system bus. Claims 12 and 13 provide similar limitations. Orr does not appear to

disclose a system where the message circuit further comprises a message pipe-line FIFO as presently claimed. Furthermore, Fletcher does not appear to disclose a system where the message circuit further comprises a message pipe-line FIFO as presently claimed.

As conceded by the Examiner, "Orr does not explicitly" disclose the additional limitations of a message circuit comprising a message pipe-line FIFO (Office Action, page 8, paragraphs 3-4). The Examiner further notes, "Fletcher does not explicitly" disclose the additional limitation of a message circuit comprising a message comprising a message pipe-line FIFO (Office Action, page 15, paragraphs 4-5). Therefore, Orr and Fletcher does not disclose a message circuit comprising a message pipe-line FIFO as in the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 3, 6-8 and 16-18 under 35 U.S.C. §103(a) as being unpatentable over Orr '350 in view of Cadambi is respectfully traversed and should be withdrawn.

The rejection of claims 3, 6-8 and 16-18 under 35 U.S.C. §103(a) as being unpatentable over Fletcher '174 in view of Cadambi is respectfully traversed and should be withdrawn.

The limitations of claim 3 were incorporated into newly amended claim 1. However, Applicants' representative disagrees with the assertion in the Office Action that "Cadambi teaches the

use of a message pipe-line FIFO" (Office Action, page 8, paragraph 5 and page 15, paragraph 6). In particular, in review of Cadambi, Cadambi fails to teach or suggest a message circuit having a message pipe-line FIFO. The Office Action asserts that the FIFO queue of Cadambi is the presently claimed message pipe-line FIFO (Office Action, page 8, paragraph 5 and page 15, paragraph 6). However, the FIFO queue of Cadambi cannot be the presently claimed message pipe-line FIFO because Cadambi fails to teach(i) a message circuit and (ii) that the message circuit further comprises a message pipe-line FIFO. The FIFO queue of Cadambi is part of the processor and not a message circuit. As noted by Cadambi, "the processor performs queuing steps of adding one marker to a First-In-First-Out (FIFO) queue **of the processor** ..." (Cadambi, column 2, lines 75-78, emphasis added). Clearly, Cadambi fails to teach or suggest both a logic circuit and a message circuit comprising message pipe-line FIFO as presently claimed. In contrast, the applicant teaches a message circuit having a message pipe-line FIFO 152 as being separate from the microprocessors 140 and 142 (see drawings, FIG. 1). Cadambi does not teach or suggest a message circuit and/or a message pipe-line FIFO as presently claimed. As such, the presently claimed invention is fully patentable over Cadambi and the rejection should be withdrawn.

With respect to claims 6 and 16, the Office Action asserts that "Cadambi teaches the control signals selected from the group consisting of (i) pipe-line overflow signals, (ii) pipe-line available signals, and (iii) command pending signals" (Office

Action, page 9, paragraph 1 and page 16, paragraph 16). However, Cadambi fails to teach or suggest the presently claimed (i) pipe-line overflow signals, (ii) pipe-line available signals and (iii) command pending signals. At best, Cadambi merely teaches the implementation of arbitration signals. No reference to the presently claimed (i) pipe-line overflow signals, (ii) pipe-line available signals and (iii) command pending signals that are generated from the message circuit is found in Cadambi. Furthermore, the arbitration signals of Cadambi are generated by a processor (see Cadambi, column 10, lines 26-30) and not by the presently claimed message circuit. Clearly, Cadambi fails to teach or suggest the presently claimed control signals selected from the group consisting of (i) pipe-line overflow signals, (ii) pipe-line available signals, and (iii) command pending signals. Furthermore, Orr and Fletcher do not cure the deficiencies of Cadambi. As such, the presently claimed invention is fully patentable over Cadambi and the rejection should be withdrawn.

Finally, with respect to pending claims 7, 8, 17 and 18, the Office Action relies on the arguments presented in support of the rejection to claim 6 to reject claims 7, 8, 17 and 18 (see Office Action, page 9, second paragraph and page 16, third paragraph). However, Cadambi fails to teach or suggest a message circuit configured to add commands written to a first address with normal priority levels and commands written to a second address with urgent priority levels. Additionally, Cadambi fails to teach or suggest that the priority levels comprise adding commands to an

end of a message queue and that the urgent priority levels comprise adding commands near to a front of the message queue. The Office Action asserts that the "priority and pipe-line discussion" of Cadambi in column 10, lines 33-57 teaches the limitations of claims 7, 8, 17 and 18 (see Office Action, page 9, paragraph 2 and page 16, paragraph 3). However, no reference to the presently claimed adding commands, normal priority levels, first and second addresses or urgent priority levels were found in the cited sections of Cadambi. Clearly, Cadambi fails to teach or suggest a message circuit configured to add commands written to a first address with normal priority levels and commands written to a second address with urgent priority levels as presently claimed. Furthermore, Cadambi fails to teach or suggest that priority levels comprise adding commands to an end of a message queue and that the priority levels comprise adding commands near to a front of a message queue as presently claimed. Neither Orr or Fletcher cures the deficiencies of Cadambi. As such, the presently claimed invention is fully patentable over Cadambi and the rejection should be withdrawn.

Dependent claims 2, 4-11 and 14-20 depend, directly or indirectly, from either claim 1 or claim 13, which are now believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Christopher P. Maiorana
Registration No. 42,829

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c/o Henry Groth
LSI Logic Corporation
1621 Barber Lane, M/S D-106 Legal
Milpitas, CA 95035

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